SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out

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Abstract

The SPIROC chip is a dedicated very front-end electronics for an ILC prototype hadronic calorimeter with Silicon photomultiplier (or MPPC) readout. This ASIC is due to equip a 10,000-channel demonstrator in 2009. SPIROC is an evolution of FLC_SiPM used for the ILC AHCAL physics prototype [1].

SPIROC was submitted in June 2007 and will be tested in September 2007. It embeds cutting edge features that fulfil ILC final detector requirements. It has been realized in 0.35m SiGe technology. It has been developed to match the requirements of large dynamic range, low noise, low consumption, high precision and large number of readout channels needed.

SPIROC is an auto-triggered, bi-gain, 36-channel ASIC which allows to measure on each channel the charge from one photoelectron to 2000 and the time with a 100ps accurate TDC. An analogue memory array with a depth of 16 for each channel is used to store the time information and the charge measurement. A 12-bit Wilkinson ADC has been embedded to digitize the analogue memory content (time and charge on 2 gains). The data are then stored in a 4kbytes RAM. A very complex digital part has been integrated to manage all theses features and to transfer the data to the DAQ which is described on [2].

After an exhaustive description, the extensive measurement results of that new front-end chip will be presented.

I. Second Generation SiPM readout: SPIROC

A. *SPIROC: an ILC dedicated ASIC.*

The SPIROC chip has been designed to meet the ILC hadronic calorimeter with SiPM readout [4]. The next figures (5 and 6) show an AHCAL scheme. One of the main constraints is to have a calorimeter as dense as possible. Therefore any space for infrastructure has to be minimized. One of the major requirements is consequently to minimize power to avoid active cooling in the detection gap. The aim is to keep for the DAQ-electronics located inside the detection gaps the power as low as 25 µW per channel.

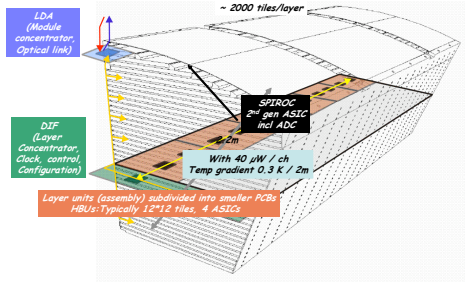


Figure 1: A half-octant of the HCAL

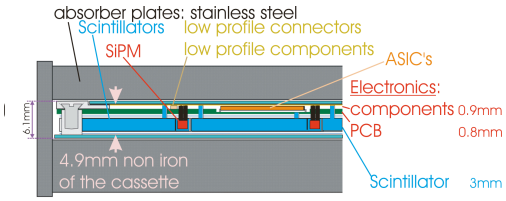


Figure 2: AHCAL integrated layer

B. *SPIROC: general description*

Table 1: SPIROC description

Technology	Austria-Micro-Systems (AMS) SiGe 0.35µm
Area	32 mm^2 (7.2mm × 4.2mm)
Power Supply	5V / 3.5V
Consumption:	25μW per channel in power pulsing mode
Package:	CQFP240 package

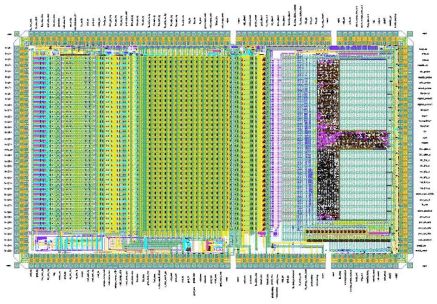


Figure 3: SPIROC layout

The SPIROC chip is a 36-channel input front end circuit developed to read out SiPM outputs. The block diagram of the ASIC is given in *Figure 4*. Its main characteristics are given in Table 1.

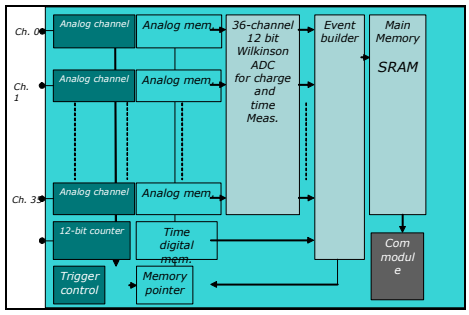


Figure 4: SPIROC general scheme

C. SPIROC analogue core

A low power 8-bit DAC has been added at the preamplifier input to tune the input DC voltage in order to adjust individually the SiPM high voltage (see *figure 5*).

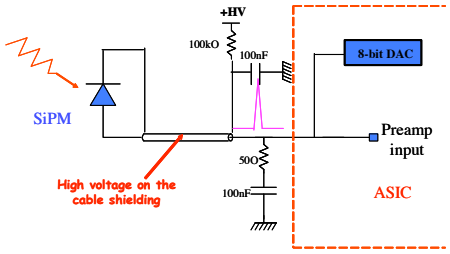


Figure 5: SPIROC connection

Two variable preamplifiers allow to obtain the requested dynamic range (from 1 to 2000 photoelectrons) with a level of noise of 1/10 photoelectron. Then, these charge preamplifiers are followed by two variable CRRC² slow shapers (50 ns-175 ns) and two 16-deep Switched Capacitor Array (SCA) in which the analogue voltage will be stored. A voltage 300 ns ramp gives the analogue time measurement. The time is stored in a 16-deep SCA when a trigger occurs. In parallel, trigger outputs are obtained via fast channels made of a fast shaper followed by a discriminator. The trigger discriminator threshold is given by an integrated 10-bit DAC common to the 36 channels. This threshold is finely tuneable on additional 4 bits channel by channel. The discriminator output feeds the digital part which manages the SCA. The complete scheme of one channel is shown on *figure 6*

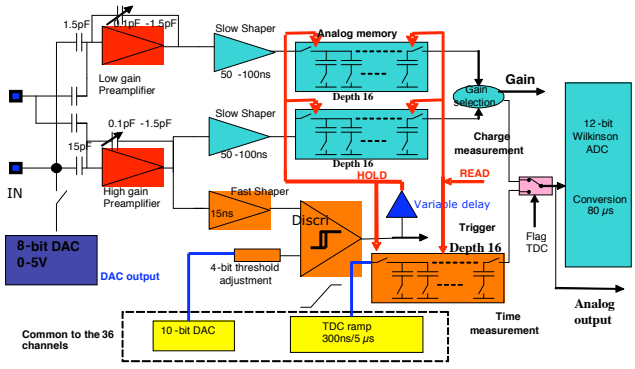


Figure 6: SPIROC one channel diagram

D. Embedded ADC

The ADC used in SPIROC is based on a Wilkinson structure. Its resolution is 12 bits. As the default accuracy of 12 bits is not always needed, the number of bits of the counter can be adjusted from 8 to 12 bits. This type of ADC is particularly adapted to this application which needs a common analogue voltage ramp for the 36 channels and one discriminator for each channel. The ADC is able to convert 36 analogue values (charge or time) in one run (about 100 μs at 40 MHz). If the SCA is full, 32 runs are needed (16 for charges and 16 for times).

E. Expected analogue performance

The new analogue chain in SPIROC allows the single photo electron calibration and the signal measurement to be on the same range, simplifying greatly the absolute calibration. An analogue simulation of a whole analogue channel is shown in *figure 7*. It is obtained with an equivalent charge of 1 photoelectron (160 fC at SiPM gain 10^6).

For the time measurement, the simulation shows a gain of 120 mV per photoelectron with a peaking time of 15 ns on the "fast channel" (preamplifier + fast shaper). The noise to photoelectron ratio is about 24 which is quite comfortable to trigger on half photoelectron.

For the energy measurement, the simulation gives a gain of 10 mV per photoelectron with a peaking time of about 100 ns on "high gain channel" (high gain preamplifier + slow shaper). The noise to photoelectron ratio is about 11 and should be sufficient for the planned application. On the "low gain channel", the noise to photoelectron ratio is about 3 and it meets largely the requirement

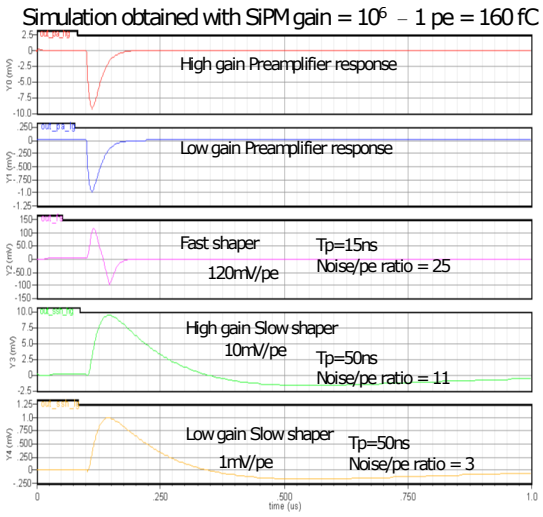
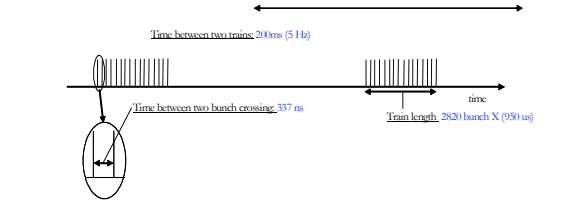


Figure 7: One channel simulation

F. SPIROC operating modes

The system on chip has been designed to match the ILC beam structure (*figure 8*). The complete readout process needs at least 3 different steps: *acquisition phase*, *conversion phase*, *readout phase*, and possibly *idle phase*.



Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

Figure 8: SPIROC running modes

- *Acquisition mode :*

During the *acquisition mode*, the valid data are stored in analogue memories in each front-end chip during the beam train. An external signal is available to erase the active column named "No_Trigger". It can be used to erase the column if a trigger was due to noise.

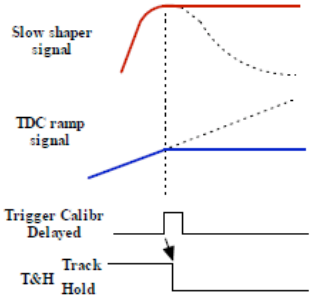


Figure 9: Operation of Track and Hold

- *Conversion mode :*

Then, during the *conversion mode*, the data are converted into digital before being stored in the chip SRAM by following the mapping represented in *figure 10*. The 36 charges and 36 times stored in SCA are converted for each column. When these 72 conversions are over, data are stored in the memory in order to start a new one for the next column.

The Bunch Crossing Identifier (BCID), hit (H) channels and gains (G) are also saved into RAM

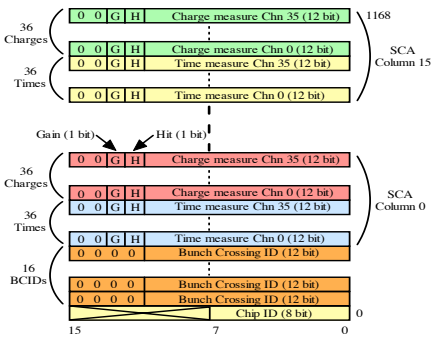


Figure 10: RAM mapping

- *Readout mode :*

Finally, during the *readout mode*, the data are sent to DAQ during the inter-train (20kbits per ASIC per bunch train). The readout is based on a daisy chain mechanism initiated by the DAQ. One data line activated sequentially is used to readout all the ASIC on the SLAB.

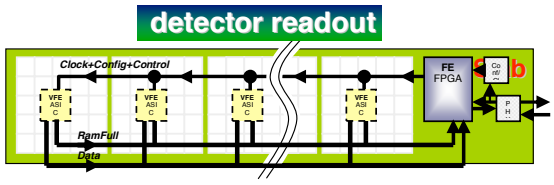


Figure 11: Detector readout scheme

- *Idle mode :*

When all these operations are done, the chip goes *to idle mode* to save power. In the ILC beam structure 99 % of power can be saved.

The management of all the different steps of normal working (acquisition, A/D measure and read-out) needs a very complex digital part which was integrated in the ASIC [3] (see on the *figure 12*).

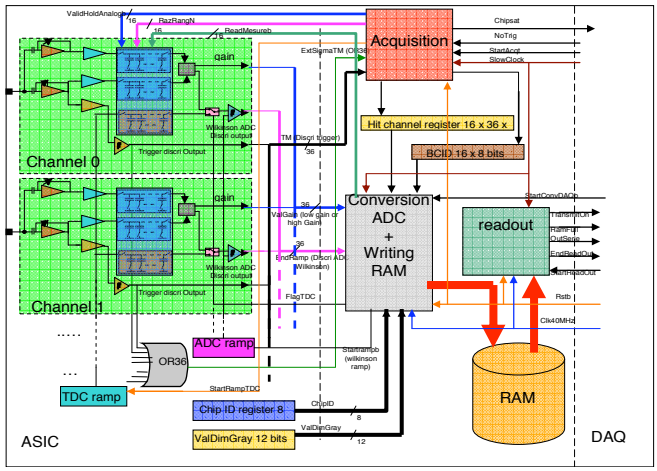


Figure 12: Interaction between digital and analog part

G. *Power pulsing*

The new electronics readout is intended to be embedded in the detector. One important feature is the reduction of the power consumption. The huge number of electronic channels makes crucial such a reduction to 25 μWatt per channel using the power pulsing scheme, possible thanks to the ILC bunch pattern: 2 ms of acquisition, conversion and readout data for 198 ms of dead time. However, to save more power, during each mode, the unused stages are off.

II. MEASUREMENTS

A. *8-bit input DAC performance*

The input DAC span goes from 4.5V down to 0.5V with a LSB of 20 mV. The default value is 4.5V in order to operate the SiPM at minimum over-voltage when the DAC is not loaded. The linearity is ±2% (5LSB), just enough for the SiPM operation but consistent with the allocated area. Also,

the dispersion between channels, although not fundamental could also be improved. The power dissipation is well within the specs and the 100nA bias current to V_{dd} makes the chip difficult to measure without special precautions.

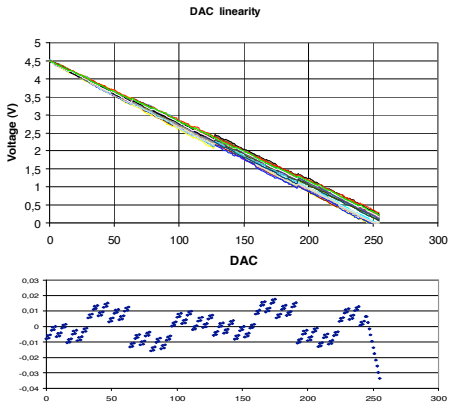


Figure 13: 8-bit DAC linearity

B. Trigger and gain selection 10-bit DAC measurement

The linearity for the two thresholds DAC was checked by scanning all the values and measuring the signal for each combination. The figure below gives the evolution of the signal amplitude as a function of the DAC combination. By fitting this line in the region without saturation (up to thermometer = 10), we obtained a nice linearity of ± 0.2 % on a large range.

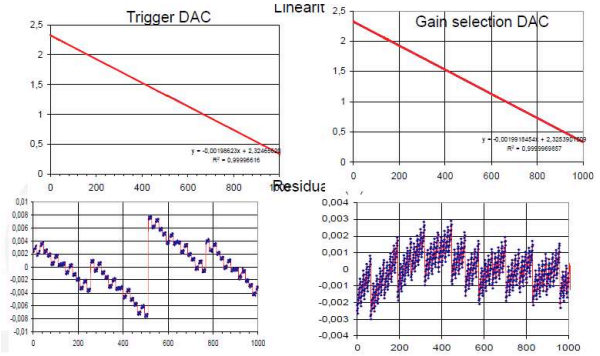


Figure 14: Trigger and gain selection 10-bit DAC linearity

C. Charge measurement

Waveforms were recorded with a fixed injected charge of 100 fC and for variable preamplifier gains as one can see on the Figure 15 which represents the amplitude as a function of time for different gains.

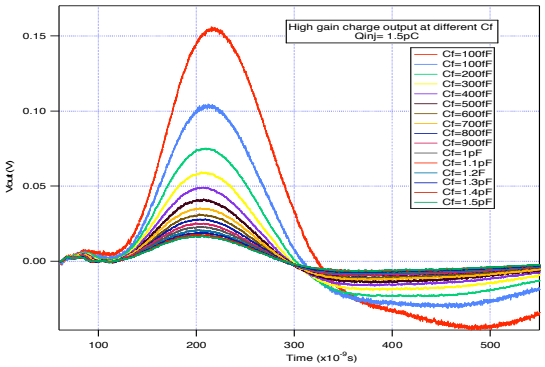


Figure 15: High gain slow shaper waveforms for a fixed injected charge of 160 fC and different preamplifier gains.

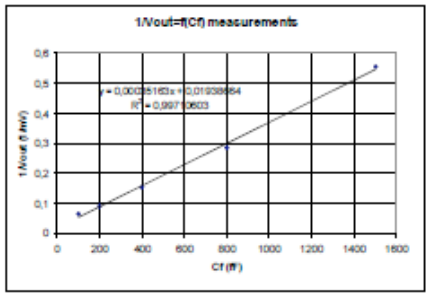


Figure 16: $1/V_{out}$ versus C_f (preamplifier gain capacitance)

From these measurements the linearity of the charge output as a function of the gain was calculated to be around ±1 % (see figure below).

The next figure represents the high gain output signal amplitude as a function of the injected charge. The fit to the linear part of the curve is better than 1%.

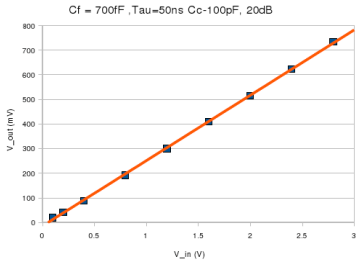
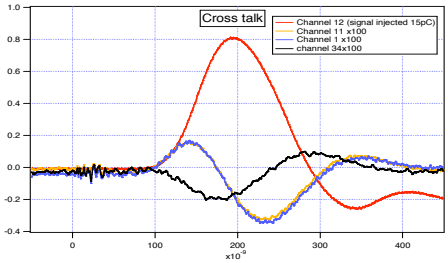


Figure 17: High gain slow shaper linearity

We also looked at the cross-talk on the slow shaper path. Figure 17 represents the waveforms of a channel 8 and its neighbours for an injected charge of 15 pC. The amplitude of the neighbouring channels is multiplied by 100. The calculation of maximum ratio gave a cross-talk of less than 0.3%. Figure 18: Cross talk



The photoelectron to noise ratio of 4 allows to nicely resolve the single photoelectrons peaks. The next figure shows the single photo electron spectrum.

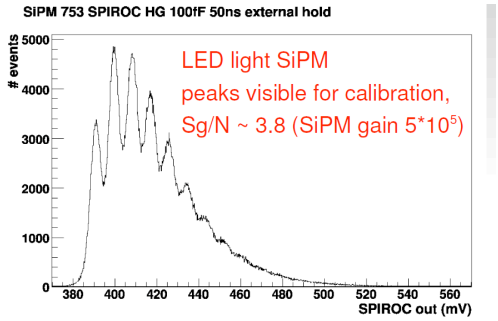


Figure 19: SiPM spectrum

D. *Time measurement*

Well known S-curves were also studied. They correspond to the measurement of the trigger efficiency during a scan of the input charge or the threshold while the other parameters, like the preamplifier gain, are kept constant. Figure 20 represents the trigger efficiency as a function of the DAC values for the 36 channels of a single chip. All channels were set at Cf=0.2pF and the input signal was fixed at Qinj=50 fC. We obtained 100 % trigger efficiency for an input charge of approximately 50 fC which corresponds to 1/3 pe as requested.

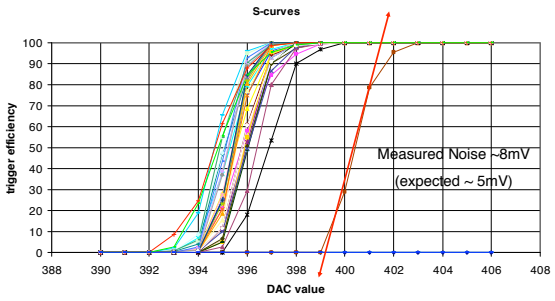


Figure 20: 36 channels S-curves

Figure 21 represents the evolution of the 50 % trigger efficiency as a function of the injected charge

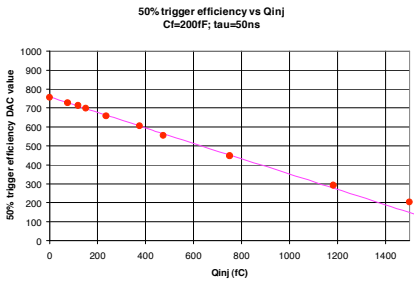


Figure 21: 50 % trigger efficiency input charge versus applied threshold for a single channel and a fixed preamplifier gain

The time walk is given on the next figure. The figure shows the relative trigger time as function of injected charge. The maximum time amplitude between small and large signal is about 10 ns.

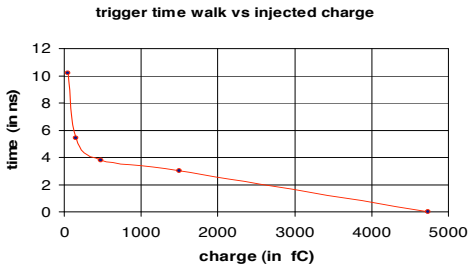


Figure 22: Time walk

III. Conclusion

The SPIROC chip has been submitted in June 2007 and its test started in October 2007. It embeds cutting edge features that fulfil ILC final detector requirements including ultra low power consumption and extensive integration for SiPM readout. The system on chip is driven by a complex state machine ensuring the ADC, TDC and memories control.

The SPIROC chip is due to equip a 10,000-channel demonstrator in 2009 in the frame work of EUDET.

IV. References

[1] LC-DET-2006-007: *Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM readout*

S. Blin[4], B. Dolgoshein[3], E. Garutti[1], M. Groll[2], C. de La Taille[4], A. Karakash[3], V. Korbel[1], B. Lutz[1], G. Martin-Chassard[4], A. Pleshk[3], L. Raux[4], F. Sefkow[1]

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[2] *DigiPtal part of SiPM Integrated Read-Out Chip ASIC for ILC hadronic calorimeter*

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[1] IN2P3/LAL, Orsay, France

[3] FLC_SIPM : *front-end chip for SIPM readout for ILC analog HCAL*

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C.De La Taille [1], G.Martin-Chassard [1], L.Raux [1]

[1] IN2P3/LAL, Orsay, France

[4] System aspects of the ILC-electronics and power pulsing

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